AMENDMENTS TO THE CLAIMS:

A detailed listing of all claims that are, or were, in the application follows:

Claims 1-15. (Cancelled)

16. (previously presented): A display element having internal optical output control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

an input configured for receiving an array position addressing signal containing array position clocking and data which are delivered in common to all said display elements within a single or multidimensional display array;

a counter configured for maintaining an array position count in response to detecting said array position clocking from said input;

a memory configured for retaining an array position;

a comparison circuit configured for generating a data load signal in response to detecting a desired relationship between said array position maintained by said counter and said array position retained in said memory;

a latch circuit configured for loading data from said input in response to receipt of said data load signal; and

a driver circuit configured for outputting said data to update the optical state of said at least one optical element.

17. (previously presented): A display element as recited in claim 16, wherein said input comprises a single signal line coupled directly to each said display element within a given display array, or a signal superimposed on the power being supplied to each said display element within said given display array.

18. (previously presented): A display element as recited in claim 16, further comprising:

a shift register coupled to said input and configured to receive data bits of said array position addressing signal in response to said data load signal;

wherein said shift register is configured to output, in parallel, the data bits it has received to said latch.

19. (previously presented): A display element as recited in claim 16, wherein said memory comprises a non-volatile memory.

20. (previously presented): A display element as recited in claim 19, wherein said memory is configured for being loaded with an array position value in response to a position programming operation.

21. (previously presented): A display element as recited in claim 16, wherein said input comprises a separate signal connection aside from the power and ground connections of said display element.

22. (previously presented): A display element as recited in claim 16, wherein said input is received as a signal superimposed over said power and ground connections to said display element.

23. (previously presented): A display element as recited in claim 16, wherein said array position clocking and data are received for each array address in each cycle of an array position addressing signal.

24. (previously presented): A display element as recited in claim 23, wherein said driver is configured for outputting said data to said at least one optical element in response to detecting the end of said cycle of said array position addressing signal.

25. (previously presented): A display element as recited in claim 16, wherein said driver circuit is configured for modulating the optical state of each of said optical elements to either an on or off state in response to said data from said latch circuit.

26. (previously presented): A display element as recited in claim 16, wherein said driver circuit is configured for modulating the optical state of each of said optical elements to a desired intensity, color, or combination of intensity and color, in response to said data from said latch circuit.

Claims 27 - 46. Cancelled

47. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for programming to a first address associated with the position of said display element within an array of said display elements;

means for extracting output data from a data signal, received in parallel by the display element and other display elements within an array of display elements, in response to matching a second address received on said data signal with said first address; and

means for modulating the output of said at least one optical element in response to said extracted output data.

48. (previously presented): A display element as recited in claim 47, wherein said first address comprises at least one axis of addressing.

49. (previously presented): A display element as recited in claim 48, wherein said first address comprises a row and column address.

50. (previously presented): A display element as recited in claim 47, wherein said means for extracting data is configured for extracting a predetermined number of data bits from said data signal.

51. (previously presented): A display element as recited in claim 50, wherein said means for extracting data is configured for counting clocks on said data signal for determining said second address.

52. (previously presented): A display element as recited in claim 51, wherein said clocks comprise column and row clocks.

53 (previously presented): A display element as recited in claim 51, wherein said means for extracting data is configured for detecting a reset clock to reset the clocks being counted in determining said second address.

54. (previously presented): A display element as recited in claim 47, wherein said data signal comprises either a single signal line coupled directly to each said display element within a given array of said display elements, or is superimposed on the power being supplied to each said display element within the array of display elements.

55. (previously presented): A display element as recited in claim 47, wherein said means for modulating the output of the optical state of said at least one optical element is configured to update the optical state of said optical element at a fixed position within cycles of said data signal.

56. (previously presented): A display element as recited in claim 55, wherein said fixed position occurs at the end of a cycle of said data signal.

57. (previously presented): A display element as recited in claim 47, wherein said means for extracting data from said common array positioning addressing signal, comprises:

a counter configured for counting clocks to determine said second address within said data signal;

an address comparator for generating a matching signal in response to detecting a predetermined relationship between said second address determined by said counter and said first address retained within said memory; and

a data store configured for collecting data bits from said data signal in response to said matching signal.

58. (previously presented): A display element as recited in claim 47, wherein said modulating means comprises:

a latch configured for latching and outputting data bits from said data store; and

a driver circuit configured for driving said at least one optical element to provide intensity, color, or combination of intensity and color, control in response to output data being output from said latch.

59. (previously presented): A display element as recited in claim 58, wherein said latch is configured to output the received data in response to a predetermined position within each cycle of the data signal.

60. (previously presented): A display element as recited in claim 47, wherein said optical element comprises one light emitting diode (LED) of a desired color, or multiple LEDs of at least one color.

61. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element;

means for extracting output control data from a data signal, received in parallel with other display elements within an array of the display elements, in response to matching a second address received from the data signal with said first address; and

means for modulating the output state of at least one said optical element in response to said extracted output control data.

62. (previously presented): A display element as recited in claim 61, further comprising means for programming said memory to said first address in response to the position of the display element within an array of the display elements.

63. (previously presented): A display element as recited in claim 62, wherein said programming means is configured for loading said second address from the data signal in response to a programming signal received by said display element and not by other display elements within an array which are not to respond to given said second address.

64. (previously presented): A display element as recited in claim 63, wherein said programming means is configured to program said second address in response to a combination of data received from said data signal and said programming signal.

65. (previously presented): A display element as recited in claim 63, further comprising an optical detector within said display element, said optical detector configured for receiving said programming signal.

66. (previously presented): A display element as recited in claim 65, wherein said optical detector comprises one or more of said at least one optical elements which are configured for both displaying optical states and detecting optical input.

67. (previously presented): A display element as recited in claim 66, wherein said optical detector comprises at least one separate optical input sensor integrated within said display element.

68. (previously presented): A display element as recited in claim 61, wherein said output control data is received on the data signal in a sequential scan form or random form.

69. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element in response to the position of the display element containing said at least one optical element within an array of said display elements;

means for extracting output control data from a common data signal received in parallel with other display elements within an array of the data elements, said output control data being extracted in response to detecting a desired relationship between said first address stored in memory and a second address received over said common data signal; and

means for modulating the output of at least one said optical element in response to said

extracted output control data.

70. (currently amended): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address, for representing the position of the display element within an array of display elements, in response to programming of said memory wherein it retains the same said first address during operation of said display element;

means for receiving a data signal in common by all display elements in an array of the display elements;

means for matching a second address received from the data signal with said first address representing display element position within an array of the display elements;

means for outputting optical state data, from said data signal for this display element position within an array of display elements, ~~received from a data signal common to all display elements in the array, to said at least one optical element~~ in response to said matching to said at least one optical element in said display element ~~a first address received from the data signal with a second address programmed within said means to the position of the display element within an array of the display elements~~.

71. (previously presented): A display element as recited in claim 70, wherein said outputting means is configured for programming said second address within said means with the display element connected in-situ on the target array.

72. (previously presented): A display element as recited in claim 70, wherein said outputting means is configured for receiving said data signal which each display element monitors within the array of display elements.

73. (previously presented): A display element as recited in claim 70, wherein said second address is programmed into non-volatile memory within said outputting means.

Claims 74 - 76. Cancelled

77. (previously presented): A display element as recited in claim 47, wherein said display element is contained within an optical housing configured with a transparent portion through which the state of said at least one optical element can be viewed.

78. (previously presented): A display element as recited in claim 47, wherein said memory is configured for storing said first address for the display element in response to a programming operation that programs the position of said display element according to its position within an array of display elements.

79. (previously presented): A display element as recited in claim 78, wherein said programming operation is performed in response to receiving an external optical programming signal while said display element is in a programming mode which loads an address received by the display element, in parallel with other display elements within an array of said display elements, as said first address into said memory.

80. (previously presented): A display element as recited in claim 79, wherein said external optical programming signal comprises an optical signal configured for establishing an array position address into each of the display elements contained within an array of display elements.

81. (previously presented): A display element as recited in claim 47, wherein said memory comprises a non-volatile memory.

82. (previously presented): A display element as recited in claim 58, wherein said driver circuit is configured for providing analog or digital intensity control.

83. (previously presented): A display element as recited in claim 47, wherein said memory, said extracting means and said modulating means are incorporated within the die of an optical element, or on an integrated circuit die to which one or more optical elements are bonded.

84. (previously presented): A display element as recited in claim 47, wherein said memory, said extracting means and said modulating means are integrated with a red, green, and blue optical element retained in said optical housing.

85. (currently amended): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element;

means for programming said memory to said first address in response to the position of the display element within an array of the display elements;

an optical detector within said display element, said optical detector configured for receiving said programming signal~~, wherein said optical detector comprises one or more of said at least one optical elements which are configured for both displaying optical states and detecting optical input~~;

~~wherein said optical detector comprises at least one separate optical input sensor integrated within said display element~~;

means for extracting output control data from a data signal, received in parallel with other display elements within an array of the display elements, in response to matching a second address received from the data signal with said first address;

wherein said programming means is configured for loading said second address from the data signal in response to a programming signal received by said display element and not by other display elements within [[an]] a same array of display elements which are not ~~to respond~~ responsive to ~~given~~ said second address; and

means for modulating the output state of at least one said optical element in response to said extracted output control data.

86. (currently amended): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for programming to a first address associated with the position of said display element within an array of said display elements;

wherein said memory is configured to retain said first address during operation until

reprogrammed to a different address;

means for programming said first address in response to optical signals coupled between said at least one optical element of the display element and an optical element contained within an external programming array configured for performing optical programming;

means for extracting output data from a data signal, received in parallel by the display element and other display elements within an array of display elements, in response to a match occurring between a second address received on said data signal to said first address; and

means for modulating the output of said at least one optical element in response to said extracted output data;

wherein said at least one optical element in said display element is controllably addressed within an array of the display elements that operates without the need of coupling row and column signal lines to the display elements.

87. (previously presented): A display element having internal control circuitry, comprising:

at least one optical element integrated within a display element configured for displaying multiple optical states;

a memory configured for storing a first address for the display element;

means for programming said first address in response to optical signals coupled between said at least one optical element of the display element and an optical element contained within an external programming array configured for performing optical programming;

means for extracting output control data from a data signal, received in parallel with other display elements within an array of the display elements, in response to matching a second address received from the data signal with said first address; and

means for modulating the output state of at least one said optical element in response to said extracted output control data.

88. (new): A display element as recited in claim 16, wherein said memory is configured to retain said array position during operation and power down of said display element and until reprogrammed to a different address.

89. (new): A display element as recited in claim 16, wherein said display element is configured for electrical connection to a base member having parallel conductive planes through which power as well as a data signal are communicating to each display element within a plurality of the display elements.

90. (new): A display element as recited in claim 16, wherein the optical elements in a plurality of said display elements are controllably addressed as an array without the need of individual row and column signal lines.

91. (new): A display element as recited in claim 47, wherein said memory is configured to retain said first address during operation and power down of said display element and until reprogrammed to a different address.

92. (new): A display element as recited in claim 47, wherein said display element is configured for electrical connection to a base member having parallel conductive planes through which power as well as a data signal are communicating to each display element within a plurality of the display elements.

93. (new): A display element as recited in claim 47, wherein the optical elements in a plurality of said display elements are controllably addressed as an array without the need of individual row and column signal lines.

94. (new): A display element as recited in claim 61:

wherein said memory is configured to retain said first address for containing the physical address for the display element within an array of the display elements; and

wherein said first address is retained during operation and power down of said display element and until reprogrammed to a different address.

95. (new): A display element as recited in claim 61, wherein said display element is configured for electrical connection to a base member having parallel conductive planes through which power as well as a data signal are communicating to each display element within a plurality

of the display elements.

96. (new): A display element as recited in claim 61, wherein the optical elements in a plurality of said display elements are controllably addressed as an array without the need of individual row and column signal lines.

97. (new): A display element as recited in claim 69, wherein said memory is configured to retain said first address during operation and power down of said display element and until reprogrammed to a different address.

98. (new): A display element as recited in claim 69, wherein said display element is configured for electrical connection to a base member having parallel conductive planes through which power as well as a data signal are communicating to each display element within a plurality of the display elements.

99. (new): A display element as recited in claim 69, wherein the optical elements in a plurality of said display elements are controllably addressed as an array without the need of individual row and column signal lines.

100. (new): A display element as recited in claim 70, wherein said memory is configured to retain said first address until reprogrammed to a different address.

101. (new): A display element as recited in claim 70, wherein said display element is configured for electrical connection to a base member having parallel conductive planes through which power as well as a data signal are communicating to each display element within a plurality of the display elements.

102. (new): A display element as recited in claim 70, wherein said at least one optical element in said display element is controllably addressed within an array of the display elements without the need of individual row and column signal lines.

103. (new): A display element as recited in claim 85, wherein said memory is configured to retain said first address during operation until reprogrammed to a different address.

104. (new): A display element as recited in claim 85, wherein said display element is configured for electrical connection to a base member having parallel conductive planes through which power as well as a data signal are communicating to each display element within a plurality of the display elements.

105. (new): A display element as recited in claim 85, wherein said at least one optical element in said display element is controllably addressed within an array of the display elements without the need of individual row and column signal lines.

106. (new): A display element having internal control circuitry, comprising:

an integrated circuit;

at least one optical element within a package of said integrated circuit, or attached to said integrated circuit and configured for displaying multiple optical states;

means for receiving power and a data signal received in parallel by said optical display unit and other optical display units within an array of optical display units;

a memory configured for programming to a first address for retaining a position value for said display element within an array of other display elements, said memory retained during operation until reprogrammed to a different address;

means for programming said first address in response to signals communicated to said display element and said other display elements within an array of said display elements for establishing said first address responsive to the position of said display element within the array of other display elements;

wherein said signals communicated by said means for programming are communicated responsive to array position of said display element within the array of display elements;

means for extracting output data from said data signal in response to a match occurring between a second address determined in response to said data signal and said first address; and

means for modulating the output of said at least one optical element of said display element in response to said extracted output data.

107. (new): A display element as recited in claim 106, wherein said data signal is superimposed on said power and received by said display element on the same two conductors which are coupled to other display elements within an associated display array.

108. (new): A display element as recited in claim 106, wherein said data signal is received as a separate signal from said power, said power and data being received by said display element on the same three conductors which are coupled to other display elements within an associated display array.

109. (new): A display element having internal control circuitry, comprising:

at least one optical element integrated within each said display element;

said display element configured for driving said at least one optical element as pixels within a display array having a plurality of pixels driven by an array of said display elements;

said optical element configured for displaying multiple optical states;

said display element configured for electrical connection to a base member having parallel conductors through which power as well as a data signal are communicating to each display element within a plurality of the display elements within a display array;

a control circuit integrated within said display element, said control circuit configured for modulating the state of said at least one optical element in response to extracting data from a serial data signal carried in parallel to said plurality of display elements;

a memory within said control circuit for retaining an array position address of the display element, within an array of display elements, which is programmed into said memory and to which this particular display element is to be responsive;

said array position address being retained during operation and power down of said display element until said display element is programmed to a different position in an array of the display elements; and

a comparison circuit within said control circuit, said comparison circuit configured for receiving the serial data signal on the parallel conductors and detecting an array position address match with said array position address retained in said memory;

said control circuit configured for extracting optical state data from said serial data signal in response to said array position address match and driving the output of said at least one optical element to said optical state; and

wherein said control circuit allows each said display element to be controllably addressed over the parallel conductors without the need of individual row and column signal lines.

110. (new): A display element as recited in claim 109, wherein said display element is configured with an electrical pinout of two or three contacts adapted for connection to a base member to which an array of the display elements can be attached.